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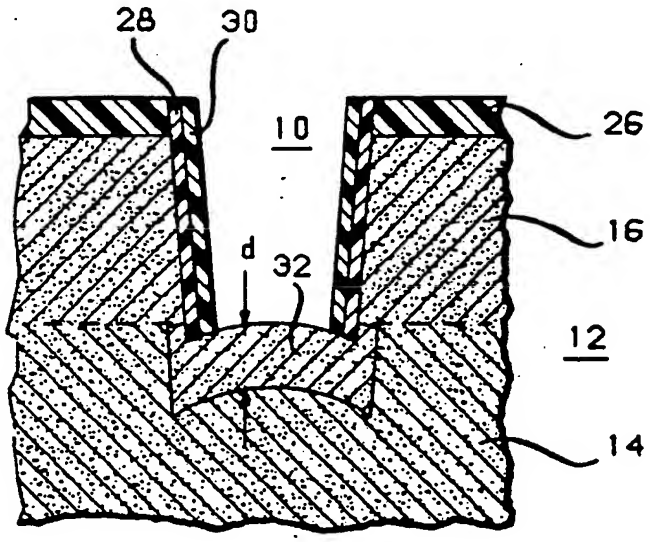

(57) Abstract

Selective wet or plasma anodization is utilized for forming a relatively thick dielectric layer (34) only at the bottoms of trenches (10) included in semiconductor, integrated devices. In that way, the electrical characteristics of trenches that include bottoms having surface roughness and/or sharp or irregular corners are significantly improved. Additionally, electrically isolated capacitor structures in elongated trenches are made feasible.

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FORMING THICK DIELECTRIC AT THE BOTTOMS OF TRENCHES UTILIZED IN INTEGRATED-CIRCUIT DEVICES

Background of the Invention

This invention relates to integrated-circuit devices and, more particularly, to a method for fabricating trenches in such devices.

It is known to utilize microminiature trenches in integrated-circuit devices for various purposes. In dynamic random-access memory (DRAM) devices, trenches having a thin dielectric layer formed on the walls and bottoms thereof serve as the basis for making high-capacitance memory cell capacitors in a relatively small area. In complementary metal-oxide-semiconductor (CMOS) devices, dielectric-filled trenches are utilized to achieve isolation between adjacent n-channel and p-channel transistor regions thereby to achieve latchup-free operation of the devices. Such isolation trenches include, for example, a composite filling including a thin high-quality dielectric formed directly on the trench walls.

In practice, the bottoms of typical trenches formed in integrated-circuit devices often exhibit imperfections such as surface roughness and/or sharp or irregular corners. In turn, these imperfections can lead to undesirable current leakage and/or voltage breakdown problems in the devices.

One solution to the problems that such imperfections cause is to form a thicker dielectric layer on the bottoms than on the sides of the trenches. But, heretofore, no satisfactory practical technique for forming such a thick dielectric has been available.

Summary of the Invention

In a silicon body including a p^+-type region, a trench if formed to expose a portion of the p^+ region at the bottom of the trench. Next, the top of the body and the sidewalls and bottom of the trench are coated with a protective layer. In an etching step, the protective layer on the bottom is then removed. Subsequently, a selective anodization procedure is carried out. In one embodiment, the exposed p^+ region at the bottom of the trench is etched and rendered porous in a wet anodization step. The porous silicon is then oxidized to form a thick layer of silicon dioxide. In another embodiment, the exposed p^+ region is selectively converted to silicon dioxide in a one-step dry anodization procedure carried out in a plasma. In either case, the protective layer on the trench sidewalls is then removed and replaced either with a thin dielectric layer or with a material that serves as a dopant source, as will be described in detail later below.

Brief Description of the Drawing

FIG. 1 shows a conventional integrated-circuit device having a standard trench formed therein;

and FIGS. 2 through 7 depict portions of an integrated-circuit device at successive stages of an illustrative trench fabrication sequence carried out in accordance with the present invention.

Detailed Description

FIG. 1 illustrates some of the problems typically encountered when a thin dielectric layer is applied to the surfaces of a microminiature trench formed in an integrated-circuit device. By way of example, FIG. 1 shows a conventional trench 10 that has dimensions a, b, and c of approximately 1.25, 4.0 and 0.5 micrometers (μm), respectively. The trench 10 is formed in a silicon body 12 that comprises a portion of a DRAM or CMOS device. The body 12 comprises, for

example, a p^+ region 14 having thereon a p-type epitaxial layer 16 having a thickness $\underline{t}$ of about 3.5 μm.

Illustratively, the walls of the trench are covered with a dielectric layer 18, e.g., a 200-Angstrom-unit (Å)-thick layer of deposited or grown silicon dioxide. The coating 18 constitutes, for example, the dielectric of a trench capacitor included in a very-large-scale-integrated (VLSI) DRAM device. In such a device, a conductive material (not shown) is utilized to provide a capacitor plate over the thin dielectric.

Alternatively, the coating 18 of FIG. 1 is designed, for example, to be the high-quality component of a two-layer dielectric utilized to form isolation trenches in a CMOS device. (For such use, the coating 18 is, for example, about 500-to-1200 Å thick). In practice, another material of lower dielectric quality (not shown) is utilized to fill the coated trench to the top. The overall dielectric properties of the resulting isolation trench are thus largely dependent on the characteristics of the thin coating 18.

A microminiature trench of the type represented in FIG. 1 often includes imperfections at the bottom thereof. These include, for example, surface irregularities 20 and/or sharp or irregular corners 22 and 24. Grown oxide layers are also thinner at the corners of silicon steps. As a result, the dielectric coating 18 often exhibits high-current-leakage and/or low-voltage-breakdown regions at these imperfections. In turn, this typically degrades the operating characteristics of the device of which the trench 10 comprises a constituent part.

By the processes of this invention, described hereinafter, a relatively thick dielectric layer is formed at the bottom of the trench 10 of FIG. 1. The aforementioned deleterious effects arising from trench-bottom imperfections are thereby avoided or

substantially alleviated.

In some integrated-circuit devices, a thick dielectric layer at the bottom of a trench is desired regardless of whether or not the trench bottom has imperfections of the type specified above. Thus, for example, in certain recently developed devices, such a thick dielectric layer at the bottom of an elongated trench is the basis for forming electrically isolated capacitors on the respective facing sidewalls of the trench. The herein-specified fabrication sequence is an attractive way of achieving such electrical isolation.

FIG. 2 shows a trench 10 made according to the present invention. A series of masking layers are initially formed on the top surface of the body 12 and on the side and bottom surfaces of the trench 10. Illustratively, these layers comprise a 1000-Å-thick layer 26 of silicon dioxide (or a suitable composite mask) formed only on the top surface of the body 12 and layers 28 and 30 overlying the layer 26 and covering all the surfaces of the trench 10. By way of example, the layer 28 comprises a 300-Å-thick layer of silicon dioxide and the layer 30 comprises a 1000-Å-thick layer of silicon nitride. Various conventional ways are known in the art for forming these layers.

Subsequently, by means of standard reactive ion etching (RIE) techniques, the top surface of the body 12 and the surfaces of the trench 10 are anisotropically etched. This is done in known ways by utilizing, for example, a plasma derived from CHF_3 for sequentially removing portions of the layers 30 and 28, respectively. Because of the near-vertical nature of the sidewalls of the trench 10, the portions of the layers 28 and 30 on the trench sidewalls are substantially unaffected during the RIE process. By contrast, the portions of the layers 28 and 30 on the top surface of the body 12 and on the bottom surface of the trench are thereby etched away. At that point, the

structure appears as shown in FIG. 3. The layer 26 remains to mask the top surface of the body 12 and portions of the layers 28 and 30 remain to mask the trench sidewalls.

Next, the exposed p^+-type region at the bottom of the trench 10 shown in FIG. 3 is anodized to render the silicon material porous. It is generally known that porous silicon can be produced by anodically biasing a silicon semiconductor in a electrolyte of hydrofluoric acid. In the present of holes at the silicon surface, silicon and hydrofluoric acid react to produce silicon fluoride and hydrogen. This reaction is enhanced for p-type silicon by illuminating the silicon surface. The removal of silicon atoms leaves dangling bonds. In turn, atoms with dangling bonds are less likely to react with the hydrofluoric acid. The etchant therefore selectively reacts with bound atoms. Ultimately, this produces a porous silicon matrix that retains much of its crystalline order even though 50-to-60 percent or even more of the silicon atoms may be etched. The porous silicon structure permits extremely rapid oxidation in the presence of oxygen at high temperatures.

According to the present invention such anodization is done, for example, in a known procedure in which about one-half of the silicon material in the affected region is removed thereby leaving a porous silicon matrix in the anodized p^+ region. Subsequently, the porous silicon is oxidized to form a silicon dioxide region.

By way of specific example, anodization is accomplished by immersing the entire device structure in an electrolyte containing, for example, 5 percent hydrofluoric acid in a 1:1 solution of acetic acid and water. The device structure is connected to the positive terminal of a d-c power supply to whose negative terminal a platinum electrode is connected. By

passing approximately 0.75 milliamperes per square centimeter through the electrolyte for about 10 minutes, the region 32 depicted in FIG. 4 is etched and rendered porous. In one example, the thickness d of the porous region 32 was approximately 2000 Å. The final density of the porous silicon is a function both of the anodic current density (more porous for higher current density) and of the initial doping of the affected region (more porous for higher p doping).

Oxidation of substantially all of the porous silicon region 32 (FIG. 4) is then carried out by exposing the device structure to oxygen in, for example, a furnace at about 900 degrees Celsius for about 5 minutes or by carrying out a rapid-thermal-annealing (RTA) step at approximately 1050 degrees Celsius for about 60 seconds. The resulting silicon dioxide region occupies about the same volume as the silicon that was anodized and made porous. As a result, the insulating region thereby formed is substantially stress-free.

Subsequently, the silicon nitride masking layer 30 (FIG. 4) on the trench sidewalls is removed by etching the depicted structure with, for example, hot phosphoric acid. The silicon dioxide layer 28 and all or part of the layer 26 are then removed from the structure by utilizing dilute HF. This also reduces the thickness of the silicon dioxide region at the bottom of the trench. At that point in the fabrication sequence, the structure appears as depicted in FIG. 5. The final thickness e of the trench-bottom oxide region 34 is approximately 1500 Å.

Alternatively, a dry rather than a wet anodization procedure can be utilized to form the trench-bottom silicon dioxide region 34 shown in FIG. 5. In the dry approach, the p^+-type bottom of the trench 10 is converted to silicon dioxide in a one-step anodization procedure carried out in a plasma. Such a dry anodization procedure involves placing the device

structure whose p^+-type regions are to be converted to silicon dioxide on an anode electrode in a plasma reaction chamber. Either oxygen or a mixture of oxygen and chlorine is introduced into the chamber. A plasma is then generated in the chamber. The properties of the resulting oxide formed on p- or p^+-type silicon portions of the structure are comparable to those of thermally grown oxide.

Further details of one-step dry anodization procedures of the type described above are set forth in "Selective Anodic Oxidation of Silicon in Oxygen Plasma" by V. Q. Ho et al, IEEE Transactions on Electron Devices, Vol. ED-27, No. 8, August 1980, pages 1436-1443, and in "Anodic Oxidation of Si in Oxygen/Chlorine Plasma" by N. Haneji et al, IEEE Transactions on Electron Devices, Vol. ED-32, No. 2, February 1985, pages 100-105. These procedures are suitable for inclusion in applicants' overall inventive process.

As stated earlier above, a structure of the type shown in FIG. 5 is useful in various recently developed devices. For some such devices, a thin dielectric layer 36 (FIG. 6) is next formed on the top surface and on the sidewalls and bottom of the trench 10. The layer 36 corresponds to the previously described layer 18 of FIG. 1. Because of the inclusion of the trench-bottom region 34 in the FIG. 6 structure, the electrical characteristics of the resulting dielectric layer 36 are substantially better than those of the layer 18 of FIG. 1. In particular, the dielectric depicted in FIG. 6 exhibits significantly improved leakage and breakdown characteristics, hence improved devices using such trenches.

As previously noted, a structure of the type shown in FIG. 5 is the basis for making devices of the type having an elongated trench in which multiple electrically isolated capacitors are formed on the respective facing sidewalls thereof. The trench-bottom

region 34 of FIG. 5 provides such isolation during fabrication steps in which a dopant source is formed in spaced-apart portions of the elongated trench. One such dopant-source portion 38 (made, for example, of phosphorus-doped silicon dioxide, so-called P-glass) is depicted in FIG. 7. During a subsequent heating step in which n-type dopant is driven from the portion 38 into the p-type sidewalls of the trench 10 as part of the capacitor fabrication procedure, the region 34 acts as a barrier to block such dopant from reaching the portion of the region 14 that underlies the region 34. In that way, effective electrical isolation is maintained between the capacitors being formed on the respective facing sidewalls 40 and 42 of the trench 10.

Although primary emphasis herein has been directed to trenches whose bottoms extend into p^+ regions of integrated-circuit device structures, the inventive process can be used with trenches which extend into non p-type material provided means are utilized to enable performance of the anodization process. Suitable such means are generally known; e.g., converting the non p-type material into p-type material, or illuminating the material in a manner to generate the holes therein necessary for the performance of the anodization process.

Claims

1. A method of fabricating an integrated-circuit device including

forming a trench in a silicon body,

CHARACTERIZED BY

forming a dielectric layer (34) at the bottom of said trench in a fabrication procedure that includes anodization.

2. A method as in claim 1 further including the step of forming a mask (26, 28, 30) on the top surface of said body and on the sidewalls of said trench, and wherein said anodization comprises a wet process in which only said trench bottom is rendered porous.

3. A method as in claim 2 wherein said porous trench bottom is then oxidized to form a relatively thick layer of silicon dioxide.

4. A method as in claim 3 wherein the region of said body at the bottom of said trench comprises p-type silicon.

5. A method as in claim 4 wherein said wet anodization process comprises immersing said body in an electrolytic bath that includes hydrofluoric acid in a solution of acid and water.

6. A method as in claim 1 further including the step of forming a mask on the top surface of said body and on the sidewalls of said trench, and wherein anodization comprises a dry process carried out in a plasma in a one-step process in which only said trench bottom is converted directly to a relatively thick layer of silicon dioxide.

7. A method as in claim 6 wherein the region of said body at the bottom of said trench comprises p-type silicon.

8. A method as in claim 5 further including the steps of

removing said mask,

and forming a relatively thin layer of silicon dioxide(36) on the sidewalls of said trench and on the bottom of said trench overlying said relatively thick layer of silicon dioxide.

9. A method as in claim 5 further including the steps of

removing said mask,

and filling at least portions of said trench with dopant-source material, said material being in contact with the sidewalls of said trench portions and overlying the relatively thick layer of silicon dioxide on the bottom of said trench portions.

10. A method as in claim 7 further including the steps of

removing said mask,

and forming a relatively thin layer of silicon dioxide on the sidewalls of said trench and on the bottom of said trench overlying said relatively thick layer of silicon dioxide.

FIG. 1
(PRIOR ART)

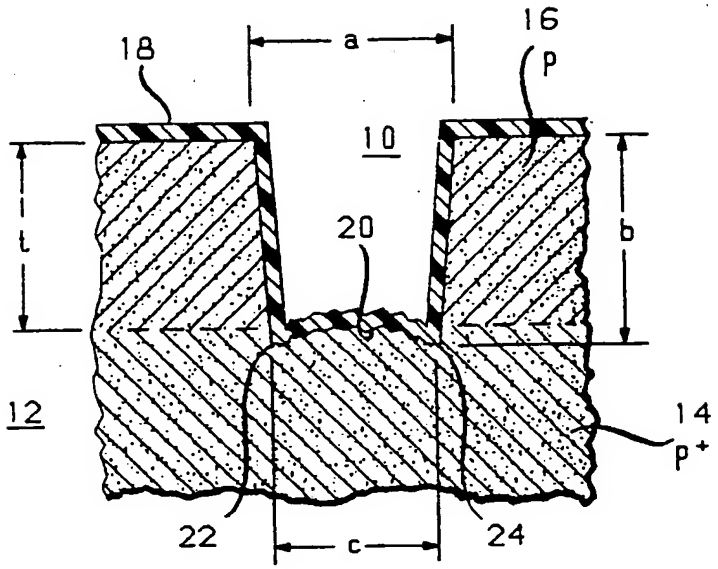


FIG. 2

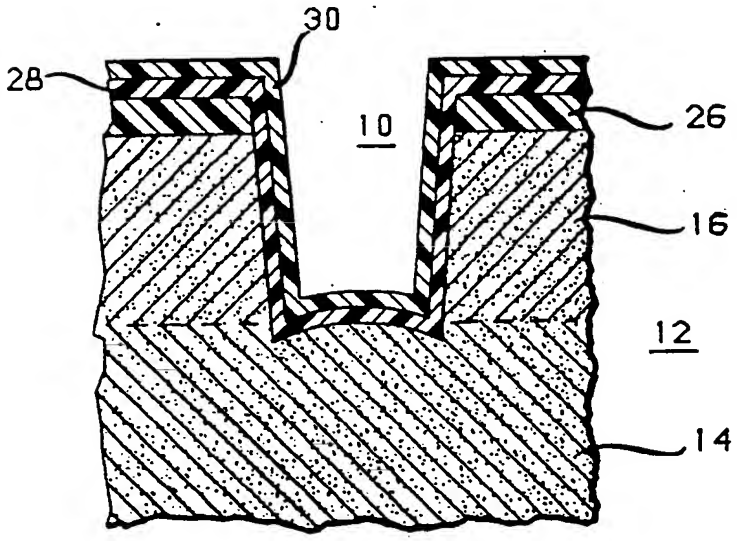


FIG. 3

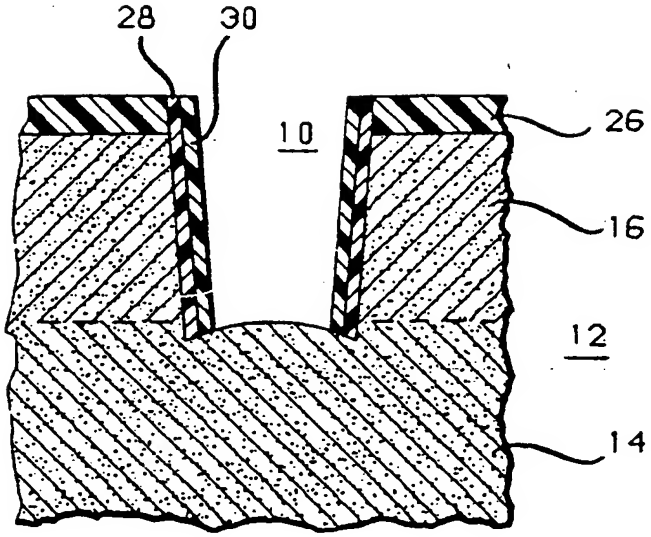


FIG. 4

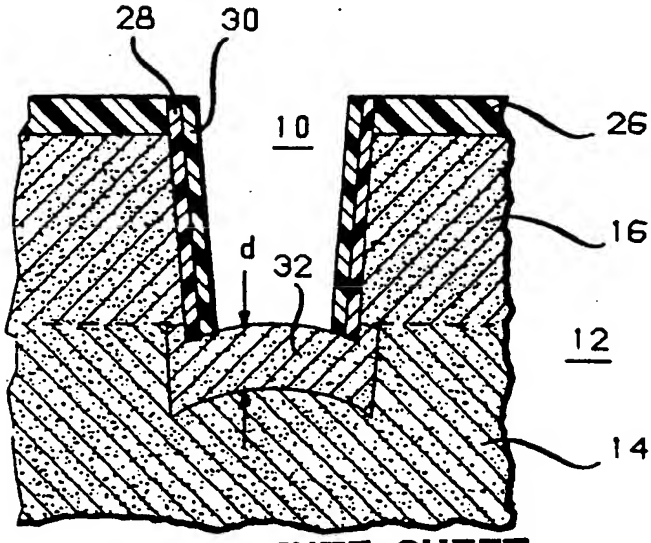


FIG. 5

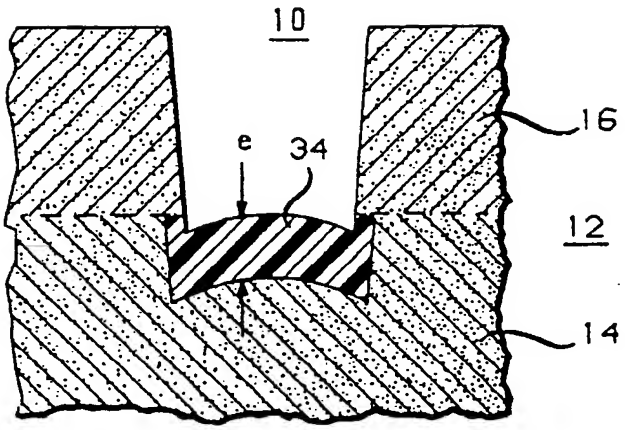


FIG. 6

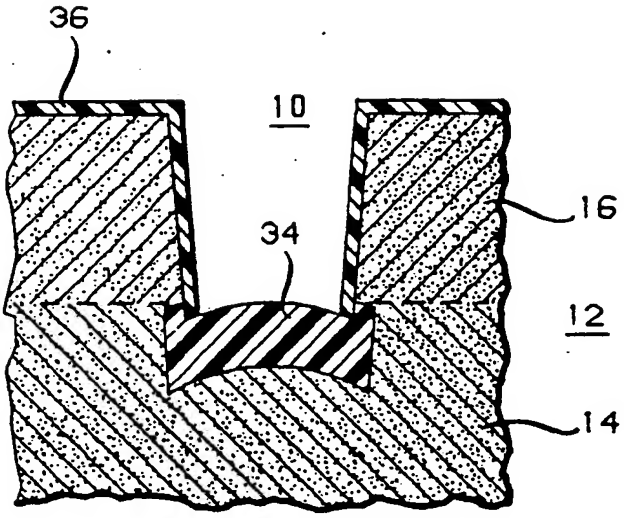
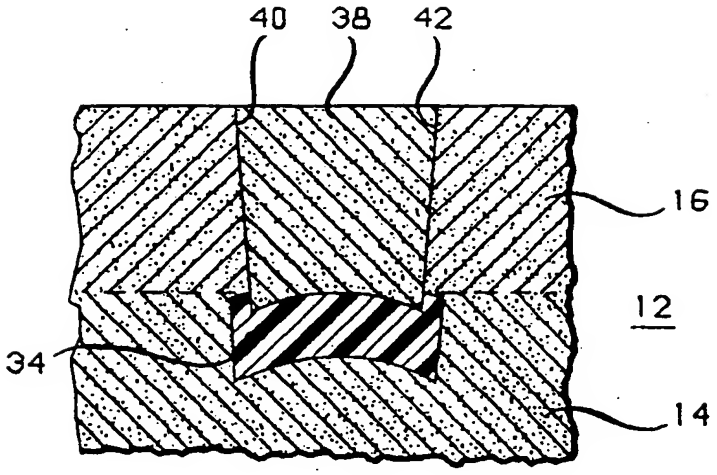


FIG. 7



INTERNATIONAL SEARCH REPORT

International Application No PCT/US 86/01472

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) *

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: H 01 L 21/306; H 01 L 21/76; H 01 L 29/94

II. FIELDS SEARCHED

Minimum Documentation Searched 7

Classification System	Classification Symbols
IPC[4]	H 01 L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are included in the Fields Searched *

III. DOCUMENTS CONSIDERED TO BE RELEVANT *

Category *	Citation of Document, 11 with indication, where appropriate, of the relevant passages 12	Relevant to Claim No. 13
X	US, A, 4459181 (J.A. BENJAMIN) 10 July 1984 see column 2, lines 1-44 --	1,3-5
A	US, A, 4104090 (H.B. POGGE) 1 August 1978 see the entire document --	1-5
A	IBM Technical Disclosure Bulletin, vol. 24, no. 11B, April 1982 (New York, US) B.M. Kemlage et al.: "Total dielectric isolation", pages 6008-6009, see figures 1-5	1-3,6-8

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* Special categories of cited documents: 10

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
17th November 1986	14 APR. 1987
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	M. VAN MOL

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/US 86/01472 (SA 13903)

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 03/12/86

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Patent document cited in search report	Publication date	Patent family member(s)		Publication date
US-A- 4459181	10/07/84	None		
US-A- 4104090	01/08/78	NL-A-	7802011	28/08/78
		FR-A,B	2382096	22/09/78
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